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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/578,440	05/25/2000	Hajime Washio	49855(904)	6115

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EXAMINER	
ABDULSELAM, ABBAS I	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/578,440	WASHIO ET AL.	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/01/04 has been entered.

2. Applicant's arguments with respect to claims 1-31 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-31 are rejected under U.S.C. 103(a) as being unpatentable over Moriyama (USPN 6232945) in view of Bi et al. (USPN 6683605) and Saito (USPN 5210712).

Regarding claims 1, 20 and 26-27, Moriyama teaches a shift register circuit containing multiple cascade-connected flip-flops in synchronization with clock signals. See col. 2, lines 40-50. Moriyama teaches a shift register circuit (21) including flip-flops, and discloses that a when a start pulse is inputted to the flip-flop 22 sub. 1, the start pulse is transferred to the succeeding stage flip-flop 22 sub.2 in synchronism with a clock pulse and output to the next step, which transmits it to the input stage switching circuit (23). See col. 15, lines 7-18 and col. 4. However, Moriyama does not teach "a plurality of level shifters such that each level shifter increases the voltage of the clock signal, and applies the clock signal to the corresponding block of flip flops" Bi on the other hand teaches a clock generator Fig. 13 (398) supplying clock signals by way of the signal level translator Fig. 14 (452). Bi discloses various clock signals (such as 32KHz and 14MHz) from a clock generator (398) are applied to the signal level translator (452) in order that suitable clock signal voltage is provided to the video controller (113A). See col. 23, lines 25-35 and col. 31, lines 25-36. Bi et al. also teaches the use of plurality of signal level translator (453, 542 and 544) as shown in Fig. 26.

Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify Moriyama's display device to include to adapt Bi's clock generator (398) along with signal level translator (452). One would have been motivated in view of the suggestion in Bi that the clock generator (398) and the signal level translator (452) are functionally equivalent to the desired level shifter. The use of clock generator (398) helps function a display system with local area networking as taught by Bi.

Moriyama does not teach, "When one or more of the blocks does not require input of the clock signal, the corresponding level shifter is suspended at that point." Saito on the other hand teaches as shown in Fig. 4 in the event when the loop is set in equilibrium state and the shift amount of the level shifter 1 becomes an appropriate amount with respect to digital signal input to the level shifter, the hold signal (stop signal) is input. As a result the shift amount of the level shifter 1 is fixed to an optimal amount. See col. 8, lines 14-25 and Fig. 4.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Moriyama's display system to adapt Saito's level shifter 1 as illustrated in Fig. 4. One would have been motivated in view of the suggestion in Saito that the level shifter 1 as configured in Fig. 4 equivalently performs the desired suspension of level shifting. The use of level shifter 1 helps function a display (127) system as taught by Saito.

Regarding claims 16, 20 and 26-27, in addition to what has been described above, Moriyama teaches a display panel section (281) including multiple pixels arranged in a matrix form. Moriyama teaches scanning line driving circuit (293) with multiple scanning lines (Y1, Y2..Yn) and video signal line driving circuit (291) with multiple video signal lines. See Fig 1. Moriyama also teaches that the scanning line driving circuit in terms of voltage application at different timing (t sub 0, t sub 1..t sub 4). See Fig 3 and col. 8, lines 12-53. Furthermore, Moriyama teaches the video signal line driving circuit that includes video signal selecting circuit (205), which outputs video signals data including non-displayed data. See col. 6, lines 32-43, col. 7, lines 54-59, 65-67, col. 8, lines 1-2 and Fig 2. Moreover, Moriyama teaches the video signal driving circuit in terms of matrix wiring section (201) and logic circuit (202) that will enable the

display data to be displayed on the pixels arranged on the (N-1) the line from the display area (502). See col. 8, lines 12-28 and Fig (1- 4).

Regarding claims 2-3, Moriyama teaches that when a pulse is inputted to the flip flop 22 sub 1 from outside, the start pulse is transferred to the succeeding stage flip-flop 22 sub 2. See col. 15, lines 10-16.

Regarding claims 4-5 and 21, Moriyama teaches a reset circuit for outputting a signal for selecting a scanning line based on the output of the flip-flop of the shift register. See col. 3, lines col. 3, lines 39-43.

Regarding claims 6 and 28, Moriyama teaches the input stage switching circuit (23) in terms of multiple flip-flops as well as pulse input and output. See col. 15, lines 7-18.

Regarding claims 7-12, 14 and 29-31, Moriyama teaches a shift register circuit (21) including flip-flops 3. Saito teaches as shown in Fig. 4 in the event when the loop is set in equilibrium state and the shift amount of the level shifter 1 becomes an appropriate amount with respect to digital signal input to the level shifter, the hold signal (stop signal) is input and as a result the shift amount of the level shifter 1 is fixed to an optimal amount. See col. 8, lines 14-25 and Fig. 4. Further Saito teaches a detector (4a) including a constant current source as well as the hold mode (HOLD) with respect to positive and negative power sources. See col. 8, lines 48-55.

Regarding claims 13 and 22-25, Bi teaches the use of plurality of signal level translators (453, 542 and 544) as shown in Fig. 26. Bi discloses a clock generator (398) with respect to signal level translator (452) in order to provide appropriate amount of clock signal voltage. See col. 23, lines 25-35 and col. 31, lines 25-36

Regarding claim 15, Moriyama teaches a display device with 853 times 480 pixels. See Fig 14. Moriyama also teaches the input staging circuit (23) as it relates to the output of the flip-flop 22 sub 107. See col. 15, lines 17-18.

Regarding claims 17-19, Moriyama teaches a display device as shown in Figure 1. See (293, 100, 121, 351) of Fig 1.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following arts are cited for further reference.

U.S. Pat. No. 5,778,237 to Yamamoto et al.

U.S. Pat. No. 6,236,260 to Vest et al.

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulselam

Examiner

Art Unit 2674

April 13, 2004

XIAO WU
PRIMARY EXAMINER